SOI INDUSTRY CONSORTIUM ANNOUNCES FOURTH ANNUAL INDUSTRY EVENT IN SILICON VALLEY TO DISCUSS SOI ADOPTION WITH SPECIAL FOCUS ON FD-SOI AND ITS APPLICATION DRIVERS

SOI symposium on April 26 in Santa Clara followed by tutorial sessions on April 27 in Milpitas

Newton, MA, April 10, 2018 – To continue showcasing the growth of the SOI ecosystem and the application drivers for ultra-low-power IC solutions, the SOI Industry Consortium, a non-profit organization representing the complete SOI-based microelectronics value chain, **has organized one day of information-sharing and networking event on April 26 and a second day targeted at RF and analog design engineers on the27th in Silicon Valley.** Activities begin at the Hyatt Regency Hotel in Santa Clara, California, with a full-day symposium – free to pre-registered attendees – to promote communication and establish connections among members of the growing SOI ecosystem. The following day, a training tutorial on designing ICs with fully depleted SOI (FD-SOI) technology focused on RF/mixed signal/ millimeter wave (mmW) will be conducted at the Crowne Plaza Hotel in nearby Milpitas, California.

The need for microelectronics that run on low power without sacrificing speed is generating increasing interest in SOI technologies. Fabless semiconductor designers, foundries and suppliers of manufacturing equipment and materials are expected to attend this year's third annual gathering to learn and discuss how to use SOI in emerging applications with a special focus on FD-SOI and its application drivers.

The program kicks off on April 26 with **two keynote addresses** by Frankwell Jyh-Ming Lin, CEO of Andes Technology, and Ron Martino, vice president and general manager of NXP Semiconductors.

A session on **"Products and Opportunities"** will follow, featuring presentations by Andre Blum of Audi, Olivier Notebaert of Airbus, Kenichi Nakano of Sony and a speaker from STMicroelectronics.

A second session on **"The Evolving SOI Ecosystem"** will include talks by Dan Hutcheson, CEO of VLSIresearch; Gregg Bartlett, senior vice president of GLOBALFOUNDRIES; Jeffrey Wang, CEO of Simgui; and an executive from Samsung's foundry business.

"Innovative Applications" will be addressed in a session featuring speakers from innovative start-ups including Ramkumar Subramanian, senior vice president of Ineda Systems; Loic Lietar, CEO of Greenwaves; Jens Benndorf, CEO of Dream Chip Technologies; Jean-Pascal Bost, CEO of eVaderis; and William Coven, CEO of Reduced Energy Microsystems.

The day will conclude with a panel discussion focusing on **"The Needs for Ultra-Low-Power Electronics and Their Application Drivers"** with panelists Wayne Dai, CEO of Verisilicon; Kelvin

Low, vice president of ARM; Timothy Saxe, CTO of QuickLogic; Mahesh Tirupattur, executive vice president of Analog Bits; and Dave Eggleston, vice president of GLOBALFOUNDRIES.

Program details and how to pre-register for free are posted at http://soiconsortium.eu/events/26-april-2018-the-annual-soi-silicon-valley-symposium-at-the-hyatt-santa-clara-ca/.

Additionally, on April 27, a training day on FD-SOI design techniques will be held at the Crowne Plaza Hotel in Milpitas, California. Organized by Andreia Cathelin of STMicroelectronics, the full-day tutorial will feature world-renowned professors and industry experts delivering a series of four training sessions dedicated to energy-efficient and low-voltage design techniques for analog, radio-frequency (RF), millimeter wave (mmW) and mixed-signal design**.**

Attendees will learn about design techniques that take full advantage of the unique features of FD-SOI, including body-biasing capabilities that further enhance FD-SOI's excellent analog/RF performance. Participants will receive concrete design examples that illustrate new implementation techniques enabled by FD-SOI technologies at the 28-nm and 22-nm nodes and beyond. Topics will cover basic building blocks through system-on-chip (SoC) applications.

Registration for the training day is $485. Early registration is advised due to limited space.

Program details and paid registration are posted at https://soiconsortium.eu/events/27-april-2018-fd-soi-training-day/.

About the SOI Industry Consortium: The SOI Industry Consortium is a non-profit organization representing the complete silicon-on-insulator (SOI)-based microelectronics value chain. The SOI Industry Consortium is chartered with promoting and supporting SOI-based technologies, a comprehensive approach to SOI ecosystems as well as innovation through application platforms. Among the activities of the SOI Industry Consortium, the association organizes industry-focused forums, workshops and training all over the world. Representing leaders from the entire electronics industry infrastructure, the SOI Industry Consortium's current 28 members include Applied Materials, ARM, Cadence Design Systems, CEA-Leti, CWS, eVaderis, GLOBALFOUNDRIES, IBM, IMEC, Incize, Invecas, NXP, Samsung, Shin Etsu Handotai, Silvaco, Simgui, SIMIT, SITRI, Soitec, Stanford University, STMicroelectronics, Surecore, Synopsys, Verisilicon, University of California Berkeley, Université Catholique de Louvain, University of Tokyo and Xpeedic. Membership is open to all companies and institutions throughout the electronics industry. For more information, please visit www.soiconsortium.org.

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